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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER

LO, L

ART UNIT

PAPER NUMBER

2614

DATE MAILED: 06/08/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/048,932

Applicant(s)

KLEIN, DEAN A.

Examiner

Linus H Lo

Art Unit

2614

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claims ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 18) ☐ Interview Summary (PTO-413) Paper No(s) ____.
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 7, 8, 10, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Dea '208.

Considering claim 1, Dea discloses a device relating to the field of video processing and in particular, to the compression and decompression of video signals. Dea discloses the following claimed subject matter, note:

1) the claimed video input port, for receiving video data for a current video frame is met by bus interface 200 (FIG. 2, column 6, lines 42-44);

2) the claimed video input buffer coupled to the video input port , for storing video data from the video input port is met by the current frame memory 204 (FIG. 2, 3A, and column 6, lines 42-44) ;

3) the claimed previous frame buffer , for storing at least a portion of a previous video frame is met by previous image memory 206 (FIG. 2, 3A and column 5, lines 38-47), wherein the described previous image block is the previous video frame;

4) the claimed operation unit coupled to the video input buffer and the previous frame buffer, for performing an operation between data from the video input buffer and data from the previous frame buffer is met by the compression/decompression accelerator 120 (FIG.

2, 3A , and column 9, line 57- column 10, line 3), whereas the described frame difference determination by the frame difference block 220 is considered as the claimed operation; and

5) the claimed result buffer coupled to the operation unit , for storing the result of an operation from the operation unit is met by the encoded data storage buffer 248(332) (FIG. 2, 3A, and column 9, line 57- column 10, line 3, column 15, lines 8-13 and column 10, line 53-column 11, line 7).

Considering claim 2, the claimed memory port coupled to the previous frame buffer and the result buffer, for transferring data to and from a memory that stores video data from the video input port and result data from the result buffer is met by bus interface 200 (FIG. 2, column 5, lines 38-47, and column 7, lines 39-44), whereas the passage from column 5 described that the memory port is coupled to the previous frame buffer, while excerpt from column 7 described the memory port is coupled to the result buffer.

Considering claim 7, note:

1) the claimed video input buffer stores a block of data from the video input port is met by the data of current image block 326 (column 6, lines 42-44 and column 10, lines 53-56);

2) the claimed previous frame buffer stores a block of data from the previous video frame is met by previous image block (column 5, lines 38-47);

3) the claimed result buffer stores a block of data from the operation unit is met by the buffer 248 (column 10, lines 53-56, and column 9, line 60- column 10, line 3); and

Art Unit: 2614

4) the claimed operation unit performs an operation between a block of data from the video input port and a block of data from the previous frame buffer is met by the description at column 9, line 60- column 10, line 3, where the frame difference block 220 is considered as the operation unit.

Considering claim 8, the claimed wherein the apparatus resides inside of a core logic chip for a computer system is met by the compress/decompression accelerator 120 that includes the function frame difference block 220 (column 6, lines 36-44, and column 5, lines 42-47, and FIG. 2).

Considering claim 10, the claimed additional resources within the apparatus, for compressing the video data from the video input port is met by the element in FIG. 2 and description at column 6, lines 36-64, where the compression/decompression accelerator 120 consists of additional resources for the purpose of compression.

Considering claim 20, claim 20 recited the same limitations as in claim 1, namely the claimed video input port, the video input buffer, the previous frame buffer, the operation unit and the result buffer, thus claim 20 is rejected for the same reason as claim 1. Additionally, the claimed central processing unit within the computer system is met by the processor 112 (FIG. 1 and column 4, lines 37-45).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3, 4, 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dea '208.

Considering claim 3, Dea discloses all the claimed limitation except for the claimed memory **coupled to the memory port** for storing the video data from the video input port and result data from the result buffer, wherein the video data is stored in a current frame area in the memory and the result data is stored in a difference frame area in the memory.

Nonetheless, Dea teaches *a memory for storing the video data from the video input port and result data from the result buffer*, wherein the video data is stored in a current frame area in the memory and the result data is stored in a difference frame area in the memory as described by memory 114 (column 10, lines 39-46, and column 11, lines 8-18), whereas the excerpt from column 10 described the video data is stored in a current frame area in the memory 114, and the passage from column 11 elucidated the result data is stored in a difference frame area in the memory 114.

Since Dea further teaches that RAM, memory, coupled to the memory port(bus interface 200) as described at column 5, lines 38-42, and it would have been obvious for one having ordinary skill to recognize that memory must be coupled to a memory port in order for the

Art Unit: 2614

contents of the memory to be read from or written into the memory location. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the cumulative features of the claimed memory **coupled to the memory port** for storing the video data from the video input port and result data from the result buffer, wherein the video data is stored in a current frame area in the memory and the result data is stored in a difference frame area in the memory in the system of Dea.

Considering claim 4, the claimed wherein the memory stores a current video frame and a previous video frame in the same location in the memory, allowing the current video frame to be written over the previous video frame is met by the description at column 12, lines 24-44, whereas the described physical buffer memory 350 which originally stores previous image and subsequently a current image is being stored in the same location in physical buffer memory 350.

Considering claim 5, the system of Dea disclose the claimed invention except for the claimed wherein the memory also stores instructions and data for a central processing unit of a computer system.

Nevertheless, Dea teaches *a memory* for the computer system in the memory as the description of DRAM 114 at column 4, lines 52-63, and furthermore Dea teaches that the video processing system 100 (computer system) utilizes executable program instructions (column 4, lines 36-51). Examiner takes Official Notice that a processing system (computer system) stores instructions for the computer system in the memory in order for the system to retrieve and

execute the programmed instruction would be within the level of one having ordinary skill in the art. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the memory also stores instructions and data for a central processing unit of a computer system in the system of Dea.

Considering claim 12, Dea discloses all the claimed limitation except for the claimed video input buffer being a register that **stores less than one video frame**.

Nonetheless, Dea teaches a video input buffer functioning as the register as described in above claim 1, and it has been held that merely recognize the difference in the storage size of a memory component would have involved a routine skilled in the art. It is well recognized that a smaller storage capacity memory device has a benefit of more cost efficiency in manufacturing which is a less expensive part than the larger size storage device.

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the well noticeable advantage as discussed above and further realize the claimed video input buffer is a register that stores less than one video frame in the system of Dea.

5. Claims 6, and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dea in view of Abramatic et al. '383.

Considering claim 6. Dea discloses the claimed invention except for the claimed limitation of wherein the operation unit performs an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer.

Nonetheless, Dea teaches that the operation unit performs *a computing of the difference frame* between data from the video input buffer and data from the previous frame buffer as discuss above in claim 1.

Additionally, Abramatic et al. teach that a form of compression consists detecting variations (difference) between one image and the next as described at column 2, lines 53-56. Abramatic et al. discloses the claimed operation unit performs an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer as met by the description at column 6, lines 52-58, whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame.

Since Abramatic et al. teach that XOR function for the difference calculation 56 which has the advantage of providing a less complicated means for the difference calculation techniques as elucidated at column 7, lines 32-35. Therefore it would have been obvious to one have ordinary skilled in the art at the time the invention was made to recognize the advantage and the claimed operation unit performs an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer as taught by Abramatic et al. in the system of Dea.

Considering claim 13, Dea discloses a device relating to the field of video processing and in particular, to the compression and decompression of video signals. Dea discloses the following claimed subject matter, note :

1) the claimed video input port, for receiving video data for a current video frame is met by bus interface 200 (FIG. 2, column 6, lines 42-44)

2) the claimed video input buffer coupled to the video input port , for storing video data from the video input port is met by the current frame memory 204 (FIG. 2, 3A, and column 6, lines 42-44) ;

3) the claimed previous frame buffer , for storing at least a portion of a previous video frame is met by previous image memory 206 (FIG. 2, 3A and column 5, lines 38-47), wherein the described previous image block is the previous video frame;

4) the claimed result buffer coupled to the operation unit , for storing the result of an operation from the operation unit is met by the encoded data storage buffer 248(332) (FIG. 2, 3A, and column 9, line 57- column 10, line 3, column 15, lines 8-13 and column 10, line 53-column 11, line 7); and

5) the claimed memory port coupled to the previous frame buffer and the result buffer, for transferring data to and from a memory that stores video data from the video input port and result data from the result buffer is met by bus interface 200 (FIG. 2, column 5, lines 38-47, and column 7, lines 39-44), wherein the passage from column 5 described that memory port coupled to previous frame buffer, while excerpt from column 7 described the memory port coupled to result buffer.

However, Dea does not explicitly disclose the following limitations , note:

a) the claimed exclusive-OR unit coupled to the video input buffer and the previous frame buffer, for performing an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer, and

b) the claimed memory coupled to the memory port for storing the video data from the video input port and result data from the result buffer, wherein the video data is stored in a current frame in the memory and the result data is stored in a difference frame in the memory.

In regarding to (a), Dea teaches that *an operation unit* coupled to the video input buffer and the previous frame for performing *a computing of the difference frame* between data from the video input buffer and data from the previous frame buffer as described by the compression/decompression accelerator 120 (FIG. 2, 3A , and column 9, line 57- column 10, line 3), whereas the described frame difference determination by the frame difference block 220 is considered as the operation;

Nonetheless, Abramatic et al. teach that a form of compression consists in detecting variations (difference) between one image and the next as described at column 2, lines 53-56. Abramatic et al. disclose the claimed exclusive-OR unit , for performing an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer as met by the description at column 6, lines 52-58, whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame.

Since Abramatic et al. teach that XOR function for the difference calculation 56 which has the advantage of providing a less complicated means for the difference calculation

Art Unit: 2614

techniques as elucidated at column 7, lines 32-35. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the advantage and the claimed exclusive-OR unit, coupled to the video input buffer and the previous frame buffer, for performing an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer as taught by Abramatic et al. in the system of Dea.

In regarding to (b), it is noted that Dea teaches *a memory for storing the video data from the video input port and result data from the result buffer*, wherein the video data is stored in a current frame area in the memory and the result data is stored in a difference frame area in the memory as described by memory 114 (column 10, lines 39-46, and column 11, lines 8-18), whereas the excerpt from column 10 described the video data is stored in a current frame area in the memory 114, and the passage from column 11 elucidated the result data is stored in a difference frame area in the memory 114.

Since Dea further teaches that RAM, memory, coupled to the memory port(bus interface 200) as described at column 5, lines 38-42, and it would have been obvious for one having ordinary skill to recognize that memory must be coupled to a memory port in order for the contents of the memory to be read from or written into the memory location. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the cumulative features of the claimed memory **coupled to the memory port** for storing the video data from the video input port and result data from the result buffer, wherein the video data is stored in a current frame area in the memory and the result data is stored in a difference frame area in the memory in the system of Dea and Abramatic et al..

Art Unit: 2614

Considering claim 14, the claimed wherein the memory stores a current video frame and a previous video frame in the same location in the memory, allowing the current video frame to be written over the previous video frame is met by the description at column 12, lines 24-44, whereas the described physical buffer memory 350 which originally stores previous image and subsequently a current image is being stored in the same location in physical buffer memory 350.

Considering claim 15, the system of Dea and Abramatic et al. disclose ~~the~~ all the claimed limitations except for the claimed limitation wherein the memory also stores instructions and data for a central processing unit of a computer system.

Nevertheless, Dea teaches *a memory* for the computer system in the memory as the description of DRAM 114 at column 4, lines 52-63, and furthermore Dea teaches that the video processing system 100 (computer system) utilizes executable program instructions (column 4, lines 36-51). Examiner takes Official Notice that a processing system (computer system) stores instructions for the computer system in the memory in order for the system to retrieve and execute the programmed instruction would be within the level of one having ordinary skill in the art. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the memory also stores instructions and data for a central processing unit of a computer system in the system of Dea and Abramatic et al. .

Considering claim 16, note:

1) the claimed video input buffer stores a block of data from the video input port is met by the data of current image block 326 of Dea (column 6, lines 42-44 and column 10, lines 53-56);

2) the claimed previous frame buffer stores a block of data from the previous video frame is met by previous image block of Dea (column 5, lines 38-47);

3) the claimed result buffer stores a block of data from the operation unit is met by the buffer 248 of Dea (column 10, lines 53-56, and column 9, line 60- column 10, line 3); and

4) the claimed exclusive-OR unit performs an exclusive-OR operation between a block of data from the video input port and a block of data from the previous frame buffer is met by the description of difference calculator performs an X-OR function at column 6, lines 52-58 of Abramatic et al., whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video blocks.

Considering claim 17, the claimed wherein the apparatus resides inside of a core logic chip for a computer system is met by the compress/decompression accelerator 120 that includes the function frame difference block 220 (column 6, lines 36-44, and column 5, lines 42-47, and FIG. 2).

Art Unit: 2614

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dea ' 208 in view of Yan '374.

Considering claim 9, Dea discloses all the claimed limitation except for the claimed wherein the apparatus comprises part of a video conferencing system .

Nonetheless, Dea teaches a compressed video data is being generated and utilized from the disclosed compression/decompression accelerator 120 as described at column 4, line 17-22. Additionally, Yan teaches the generated compressed video signal that is commonly having the application in videophone, video conference and other audio-visual transmission over networks as described at column 3, lines 52-64, and which immanently consists part of a video conference system.

Since Dea recognizes a compressed video data is being generated and utilized as described above, and further Yan additionally demonstrated the compressed video data has an applications in the usage of video conference which would have be immanently consists part of a video conference system. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the claimed apparatus which comprises part of a video conferencing system as taught by Yan in the system of Dea , in order to recognize the benefit of bandwidth conservation of compressed video data in the usage of video conferencing.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dea '208 in view of Hardiman ' 223.

Considering claim 11, Dea discloses all the claimed limitations except for the claimed color space conversion circuit coupled between the video input port and the video input buffer.

Hardiman discloses an invention which relates to compression coding of a video program. Hardiman discloses the claimed color space conversion circuit coupled between the video input port and the video input buffer is met by the subsampler and color space converter 80 (column 3, lines 47-57, column 6, lines 55-64, and FIG. 2), where the described video data/bus and the subsample FIFO are considered as the video input port and buffer, respectively.

Since it was well known in the art that the color space conversion on video would recognize the benefit of properly converting the video information from a computer processed information into a displayable signal for image displaying (column 3, lines 47-57). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the advantage of performing a color space conversion on the video data and further realize claimed color space conversion circuit coupled between the video input port and the video input buffer as taught by Hardiman in the system of Dea.

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the system of Dea and Abramatic et al. as applied to claim 13 above, and further in view of Yan '374.

Considering claim 18, the system of Dea and Abramatic et al. disclose all the claimed limitations except for the claimed wherein the apparatus comprises part of a video conferencing system.

Nonetheless, Dea teaches a compressed video data is being generated and utilized from the disclosed compression/decompression accelerator 120 as described at column 4, line

17-22. Additionally, Yan teaches the generated compressed video signal that is commonly having the application in videophone, video conference and other audio-visual transmission over networks as described at column 3, lines 52-64, and which immanently consists part of a video conference system.

Since Dea recognizes a compressed video data is being generated and utilized as described above, and further Yan additionally demonstrated compressed video data has an applications in the usage of video conference which would have be immanently consists part of a video conference system. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the claimed apparatus comprises part of a video conferencing system as taught by Yan in the system of Dea and Abramatic et al. , in order to recognize the benefit of bandwidth conservation of compressed video data in the usage of video conferencing.

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over the system of Dea and Abramatic et al. as applied to claim 13 above, and further in view of Hardiman ' 223.

Considering claim 19, the system of Dea and Abramatic et al. disclose all the claimed limitations except for the claimed **color space conversion circuit** coupled between the video input port and the video input buffer.

Hardiman discloses an invention which relates to compression coding of a video program. Hardiman discloses the claimed color space conversion circuit coupled between the video input port and the video input buffer is met by the subsampler and color space converter 80 (column 3, lines 47-57, column 6, lines 55-64, and FIG. 2), where the described video

data/bus and the subsample FIFO are considered as the video input port and buffer, respectively.

Since it is well known in the art that the color space conversion on video would be recognized the benefit of properly converting the video information from a computer processed information into a displayable signal for image displaying (column 3, lines 47-57). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the advantage of performing a color space conversion on the video data and further realize the claimed color space conversion circuit coupled between the video input port and the video input buffer as taught by Hardiman in the system of Dea and Abramatic et al..

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakaya et al. disclose a system and method for performing video coding/decoding using motion compensation.

Jung discloses an apparatus for detecting motion vectors using moving object patterns.

Ersoz et al. disclose a displaying an interlaced video signal with a noninterlaced video signal.

Yoshida discloses an image processing apparatus and method .

Lee discloses an apparatus for detecting a foreground region for use in a low bit-rate image signal encoder.

Sahrraray discloses method for detecting camera -motion induced scene changes.

Art Unit: 2614

Pirson et al. disclose a method for selecting motion vectors and image processing device implementing the said method.

Wu et al. disclose a system and method for enforcing interlaced field synchronization in the presence of broken alternation in an MPEG video data stream.

Kopet et al. disclose a motion estimation coprocessor.

Werner discloses an integrated MPEG decoder and image resizer for SLM-based digital display system.

11. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications intended for entry) and (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II,
2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Art Unit: 2614

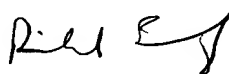
12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linus H. Lo whose telephone number is (703) 305-4039. The examiner can normally be reached on Monday-Thursday from 8:30 am to 6:00 pm. The examiner can also be reached on alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reinhard Eisenzopf can be reached on (703) 305-4711. The fax phone number for this Group is (703) 308-5359.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

lhl LL

May 29, 2001


REINHARD J. EISENZOPF 6-4-01
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600